



MSM82000CB - 015/020

Issue 1.0 March 2002

2M x 8 Static RAM

Description

The MSM82000CB is a 2M x 8 SRAM device available in Chip Size BGA (Ball Grid Array) package, with access times of 15 and 20ns. The device is available to commercial and industrial temperature grades.

The Chip Size BGA provides an ultra high density memory packaging solution.

The Chip Size BGA occupies less than 50% of the board area of conventional SOP, SOJ and TSOP II packages.

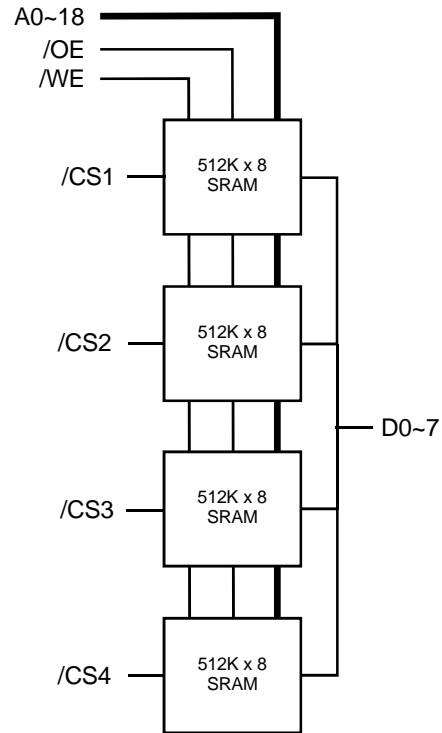
Features

- Access times of 15/20 ns.
- 5V \pm 10%
- Commercial & Industrial temperature grades
- Chip Size BGA.
- 48 ball 6x8 matrix, 1mm pad pitch.
- Eutectic 63/67 solder ball attach.
- Low Power Dissipation.
 - Operating 2 W (max)
 - Standby (CMOS) 330mW (max)
- Completely Static Operation.
- 2 layer BT substrate.
- Pinout and footprint will remain the same in the event of a die shrink.

Package Details

48D - 48 Ball, 1mm pitch Chip Size BGA
Max. Dimensions (mm) - 10.00 x 8.00 x 1.40

Block Diagram



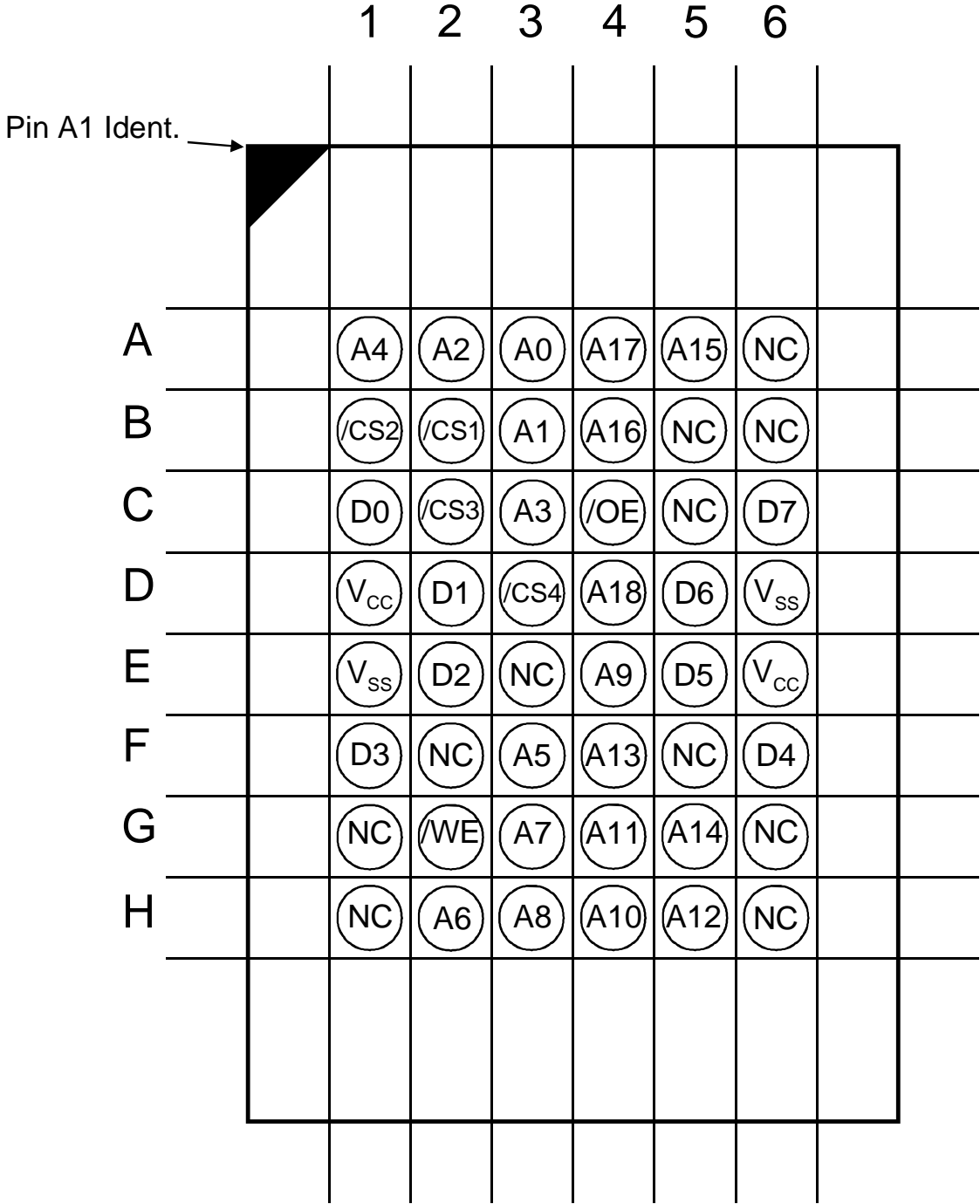
Pin Definition

See page 2.

Pin Functions

Description	Signal
Address Input	A0~A18
Data Input/Output	D0~D7
Chip Select	/CS1~4
Write Enable	/WE
Output Enable	/OE
No Connect	NC
Power	V _{CC}
Ground	GND

Pinout (Top View)



Note : Pinout shows top view,
balls facing down.

Absolute Maximum Ratings⁽¹⁾

Parameter	Symbol	Min		Max	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5	to	+7.0	V
Power Dissipation	P_T			2	W
Storage Temperature	T_{STG}	-55	to	+150	$^{\circ}C$

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2	-	$V_{CC}+0.5$	V	
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	
Operating Temperature	T_A	0	-	70	$^{\circ}C$	
	T_{AI}	-40	-	85	$^{\circ}C$	(I Suffix)

DC Electrical Characteristics

($V_{CC}=5V \pm 10\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN}=V_{SS}$ to V_{CC}	-8	-	8	μA
Output Leakage Current	I_{LO}	$/CS=V_{IH}$ or $/OE=V_{IH}$ or $/WE=V_{IL}$, $V_{OUT}=V_{SS}$ to V_{CC}	-8	-	8	μA
Operating Supply Current	I_{CC1}	Min. Cycle, 100% Duty $/CS=V_{IL}$, $V_{IN}=V_{IH}$ or V_{IL} , $I_{OUT}=0mA$	-	-	360	mA
Standby Supply Current	I_{SB}	Min. Cycle, $/CS=V_{IH}$	-	-	240	mA
	I_{SB1}	$f=0MHz$, $CS \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	-	-	60	mA
Output Voltage	V_{OL}	$I_{OL}=8.0mA$	-	-	0.4	V
	V_{OH}	$I_{OH}=-4.0mA$	2.4	-	-	V

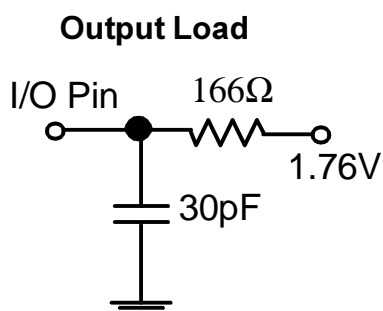
Capacitance

($V_{CC} = 5.0V \pm 10\%$ $T_A = 0^\circ C$ to $70^\circ C$)

Parameter	Symbol	Test Condition	Typ	max	Unit
Input Capacitance	C_{IN}	$V_{IN}=0V$	-	40	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}=0V$	-	40	pF

Test Conditions

- Input pulse levels : 0V to 3.0V
- Input rise and fall times : 3ns
- Input and Output timing reference levels : 1.5V
- Output Load : See Load Diagram.
- $V_{CC} = 5V \pm 10\%$



Functional Description

/CS1	/CS2	/CS3	/CS4	/WE	/OE	Mode	I/O Pin	Supply Current
H	H	H	H	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	X	X	X	H	H	Output Disable	High-Z	I_{CC}
L	H	H	H	H	L	Read	D_{OUT}	I_{CC}
H	L	H	H	H	L	Read	D_{OUT}	I_{CC}
H	H	L	H	H	L	Read	D_{OUT}	I_{CC}
H	H	H	L	H	L	Read	D_{OUT}	I_{CC}
L	H	H	H	L	X	Write	D_{IN}	I_{CC}
H	L	H	H	L	X	Write	D_{IN}	I_{CC}
H	H	L	H	L	X	Write	D_{IN}	I_{CC}
H	H	H	L	L	X	Write	D_{IN}	I_{CC}

Note : X = Don't Care

The above describes valid operating modes of the device. The use of any other operating modes described above may damage the device.

Read Cycle

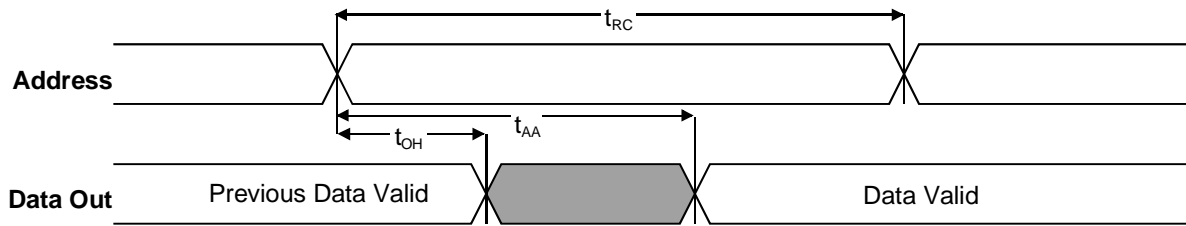
		015		020		
Parameter	Symbol	Min	Max	Min	Max	Units
Read Cycle Time	t_{RC}	15	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	20	ns
Chip Select Access Time	t_{CO}	-	15	-	20	ns
Output Enable to Output Valid	t_{OE}	-	7	-	9	ns
Output Hold From Address Change	t_{OH}	3	-	3	-	ns
Chip Selection to Output in Low Z ⁽⁴⁾	t_{LZ}	3	-	3	-	ns
Output Enable to Output in Low Z ⁽⁴⁾	t_{OLZ}	0	-	0	-	ns
Chip Deselection to Output in High Z ⁽³⁾	t_{HZ}	0	7	0	9	ns
Output Disable to Output in High Z ⁽³⁾	t_{OHZ}	0	7	0	9	ns

Write Cycle

		015		020		
Parameter	Symbol	Min	Max	Min	Max	Units
Write Cycle Time	t_{WC}	15	-	20	-	ns
Chip Selection to End of Write	t_{CW}	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	12	-	15	-	ns
Address Setup Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	10	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	7	0	9	ns
Data to Write Time Overlap	t_{DW}	7	-	9	-	ns
Data Hold time from Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}	3	-	3	-	ns

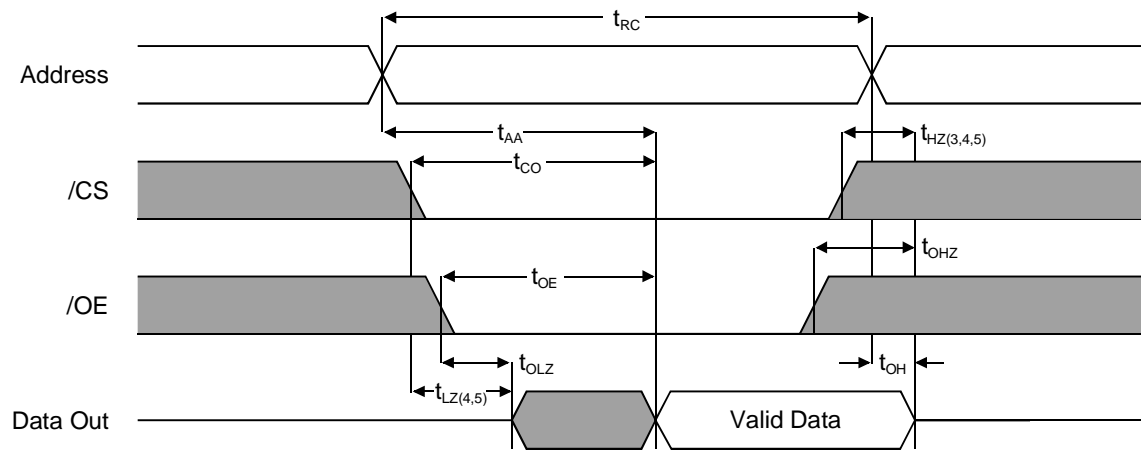
Read Cycle 1

(Address Controlled, /CS=/OE= V_{IL} , /WE= V_{IH})



Read Cycle 2

(/WE = V_{IH})

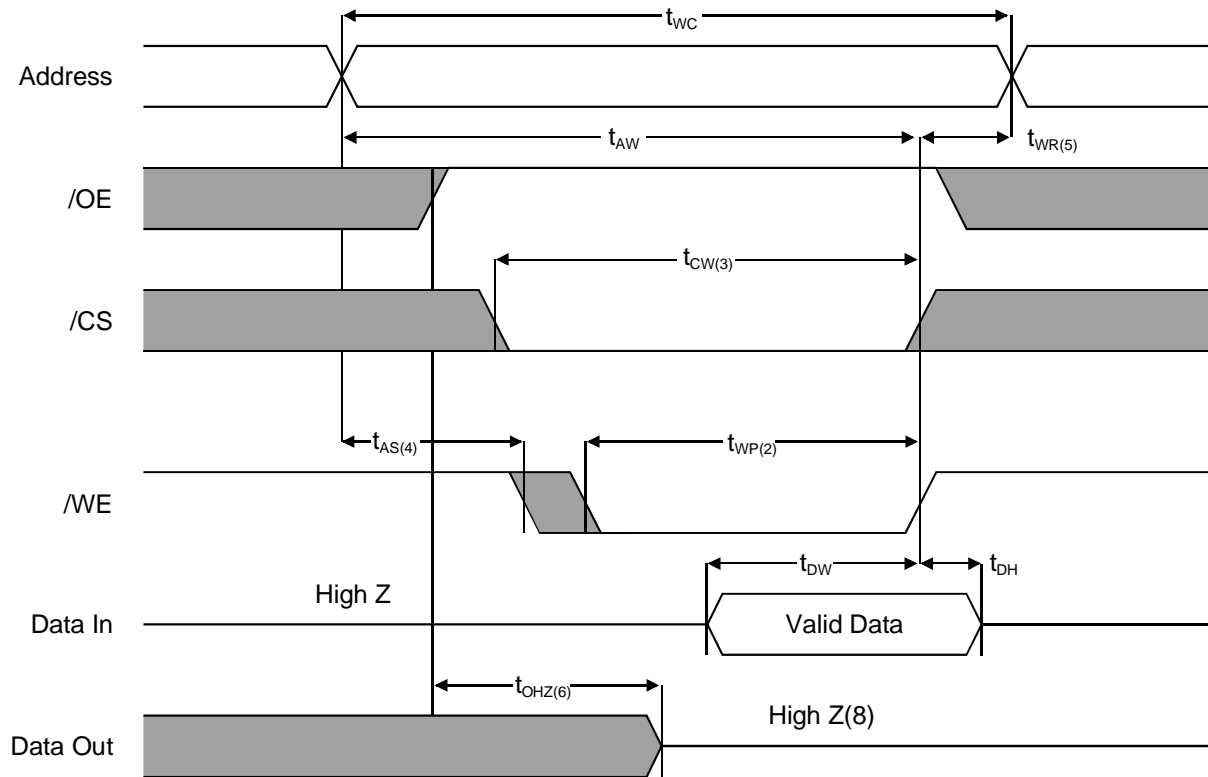


NOTES(READ CYCLE)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CS= V_{IL} .
7. Address valid prior to coincident with /CS transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

Write Cycle 1

(/OE = Clock)

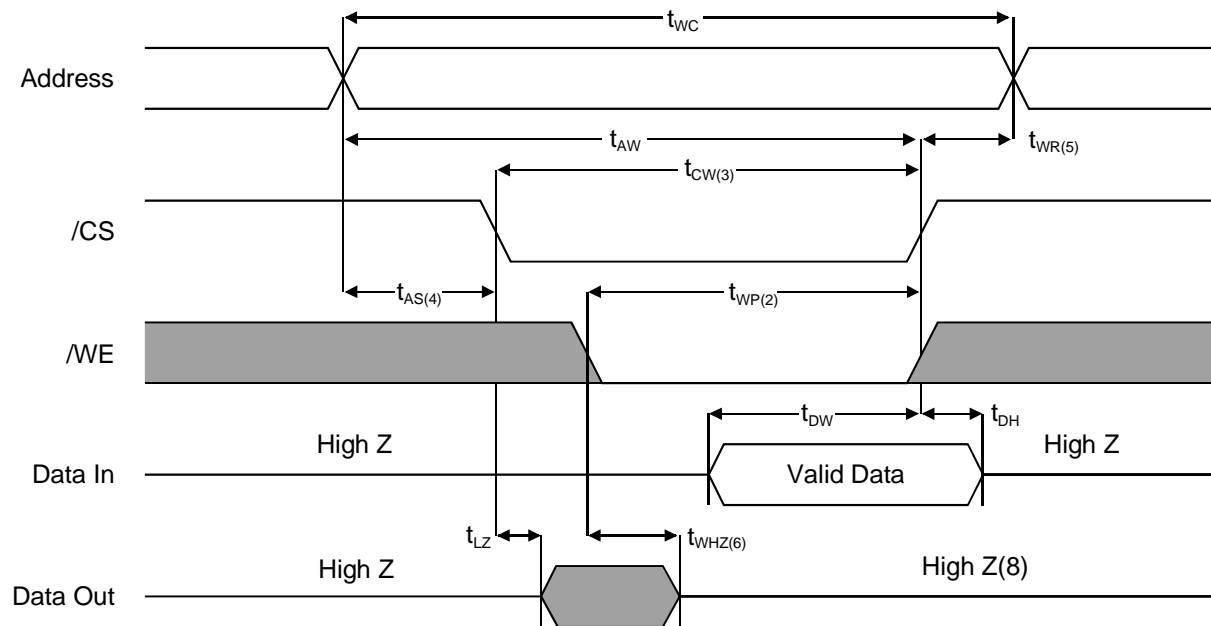


NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Write Cycle 3

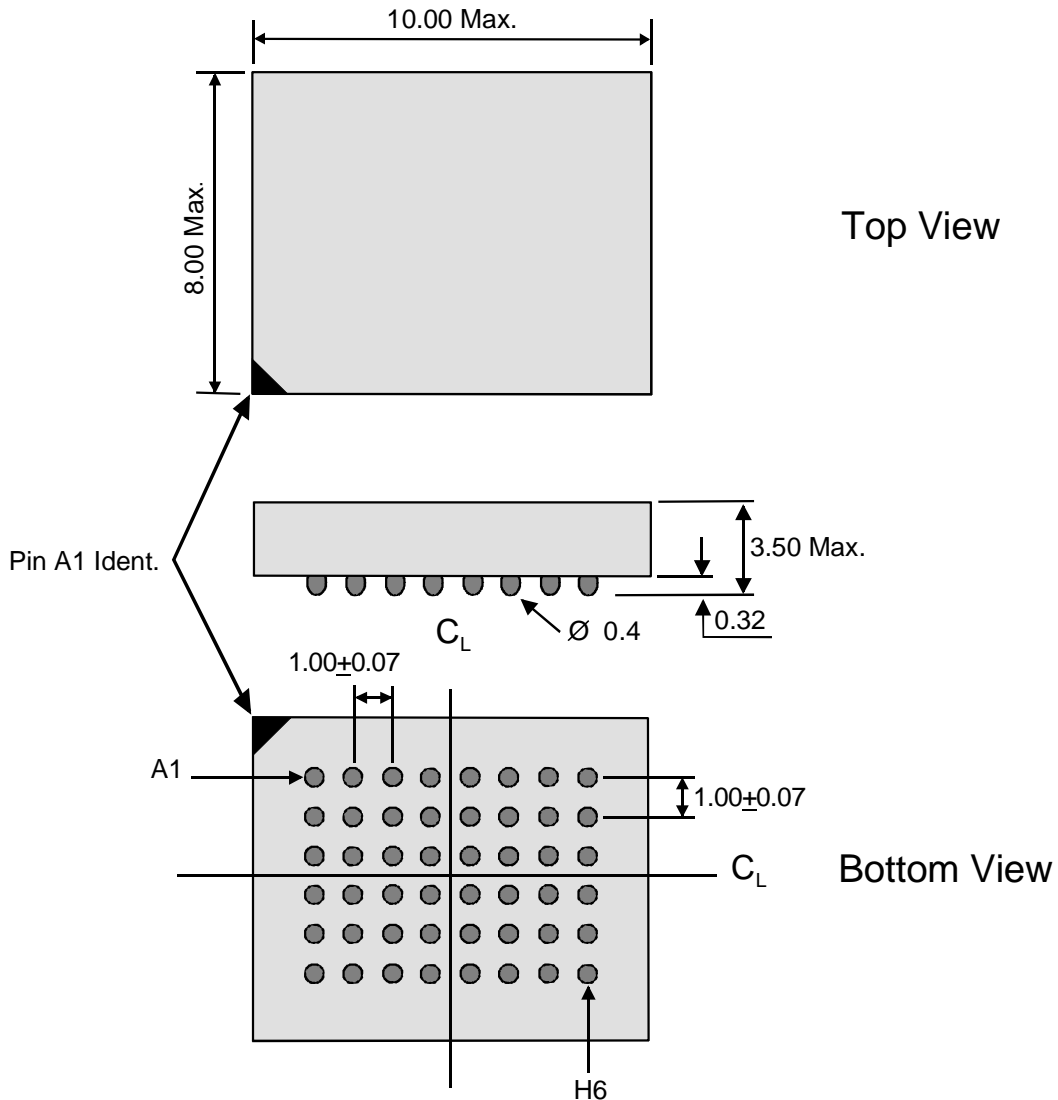
(/CS = Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Chip Size BGA - 48 pad



General Reliability Data	
High Temperature Operating Life	125°C / 6V 1000hrs
High Temperature Storage Life	150°C / 1000hrs
Autoclave	121°C / 100% RH / 168hrs
Temperature Cycling	-55 ~ 125°C / 1000 cycles
Moisture Sensitivity	JEDEC Level3 30°C / 60% RH / 192hrs
°JA Thermal Performance	30 ~ 45°C/Watt

