

# TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES

# hmp

## 256K x 32 SRAM

### MS32256FKX-35/45/55

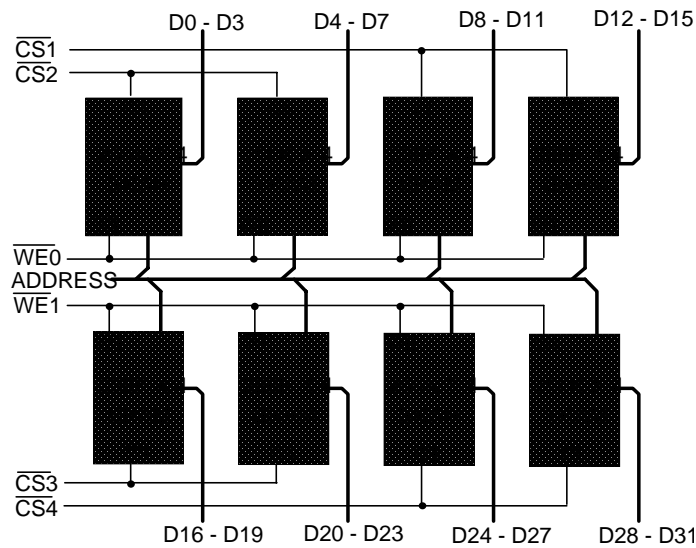
Issue 1.1 : October 1990

262,144 x 32 CMOS High Speed Static RAM

#### Features

- Very Fast Access Times of 35/45/55 ns.
- 60 Pin 0.6" DIP Package.
- Output Configurable as 32 / 16 / 8 bit
- Operating Power 2.8 / 2.0 / 1.6 W (typ).
- Low Power Standby 800  $\mu$ W (typ).
- 160  $\mu$ W (typ) -L Version.
- Completely Static Operation.
- Equal Access and Cycle times.
- Battery back-up capability.
- Directly TTL compatible.

#### Block Diagram



#### Pin Definition

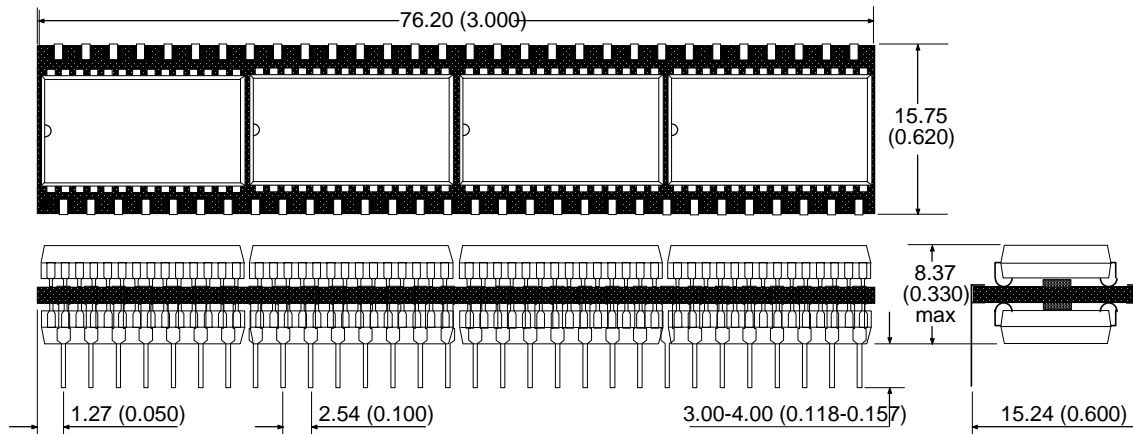
V <sub>cc</sub>	1	60	GND
A0	2	59	D31
D0	3	58	D30
D1	4	57	D29
D2	5	56	D28
D3	6	55	A17
CS1	7	54	A16
A1	8	53	CS4
D4	9	52	D27
D5	10	51	D26
D6	11	50	D25
D7	12	49	D24
A2	13	48	A15
A3	14	47	A14
WE0	15	46	WE1
A4	16	45	A13
A5	17	44	A12
D8	18	43	D23
D9	19	42	D22
D10	20	41	D21
D11	21	40	D20
A6	22	39	A11
A7	23	38	A10
CS2	24	37	CS3
D12	25	36	D19
D13	26	35	D18
D14	27	34	D17
D15	28	33	D16
A8	29	32	A9
GND	30	31	V <sub>cc</sub>

#### Pin Functions

- A0-A17** Address Inputs
- D0-31** Data Inputs/Outputs
- CS1-4** Chip Selects
- WE0-1** Write Enables
- V<sub>cc</sub>** Power
- GND** Ground

#### Package Details

Dimensions in mm (inches) Tolerance on all dimensions  $\pm 0.254(0.010)$ .



**Absolute Maximum Ratings**<sup>(1)</sup>

Voltage on any pin relative to GND	$V_{IN}$	-0.5 to +7.0	V
Power Dissipation	$P_D$	5.5	W
Storage Temperature	$T_{STG}$	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.  
 (2) Pulse width:- 2.0 V for less than 10ns.

**Recommended Operating Conditions**

		<i>min</i>	<i>typ</i>	<i>max</i>	
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.2	-	$V_{CC}+0.5$	V
Input Low Voltage	$V_{IL}$	-0.5	-	0.8	V
Operating Temperature	$T_A$	0	-	70	°C
	$T_{AI}$	-40	-	85	°C (I Suffix)

**DC Electrical Characteristics** ( $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $V_{CC} = 5V \pm 10\%$ )

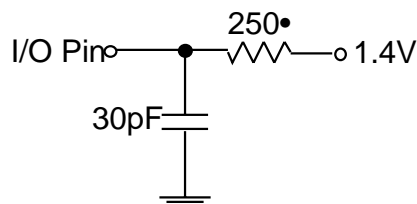
Parameter	Symbol	Test Condition	<i>min</i>	<i>typ</i> <sup>(1)</sup>	<i>max</i>	Unit
Input Leakage Current	A0-A17	$I_{L11}$ $V_{CC}=5.5V, V_{IN}=GND$ to $V_{CC}$	-	-	16	$\mu A$
	$\overline{WE0}, \overline{WE1}$	$I_{L12}$ As above	-	-	8	$\mu A$
	$\overline{CS1}-\overline{CS4}$	$I_{L13}$ As above	-	-	4	$\mu A$
Output Leakage Current	8 BIT	$I_{LO}$ $\overline{CS}'s = V_{IH}, V_{OUT} = GND$ to $V_{CC}$	-	-	8	$\mu A$
Operating Supply Current	32 BIT	$I_{CC32}$ $\overline{CS}'s = V_{IL}, I_{I/O} = 0mA$ , min. cycle	-	560	960	mA
	16 BIT	$I_{CC16}$ As above	-	400	720	mA
	8 BIT	$I_{CC8}$ As above	-	320	600	mA
Standby Supply Current	TTL	$I_{SB1}$ $\overline{CS}'s = V_{IH}$	-	240	480	mA
	CMOS	$I_{SB2}$ $\overline{CS}'s \cdot V_{CC} - 0.2, 0.2V \cdot V_{IN} \cdot V_{CC} - 0.2V$	-	0.16	16	mA
	-L Part CMOS	$I_{SB3}$ As above	-	32	1600	$\mu A$
Output Low Voltage	$V_{OL}$	$I_{OL} = 4.0 mA$	-	-	0.4	V
Output High Voltage	$V_{OH}$	$I_{OH} = -4.0 mA$	2.4	-	-	V

Note (1) Typical limits are  $V_{CC} = 5.0V$  and  $T_A = 25^{\circ}C$  and specified loading

**Capacitance** ( $T_A = 25^{\circ}C, f = 1MHz$ )

Parameter	Symbol	Test Condition	<i>typ</i>	<i>max</i>	Unit
Input Capacitance	A0 - A17,	$C_{IN1}$ $V_{IN} = 0V$	-	48	pF
	$\overline{WE0}, \overline{WE1}$	$C_{IN2}$ $V_{IN} = 0V$	-	24	pF
	$\overline{CE0} - \overline{CE3}$	$C_{IN3}$ $V_{IN} = 0V$	-	12	pF
Input/Output Capacitance:	8 BIT	$C_{I/O8}$ $V_{OUT} = 0V$	-	44	pF
	16 BIT	$C_{I/O16}$ $V_{OUT} = 0V$	-	22	pF
<b>AC Test Conditions</b>	32 BIT	$C_{I/O32}$ <b>Output Load</b>	-	11	pF

- \* Input pulse levels: GND to 3.0V
- \* Input rise and fall times: 5ns
- \* Output Load : See Load Diagram
- \* Input/Output timing reference levels: 1.5V
- \* MS32256 tested in 32 bit mode.

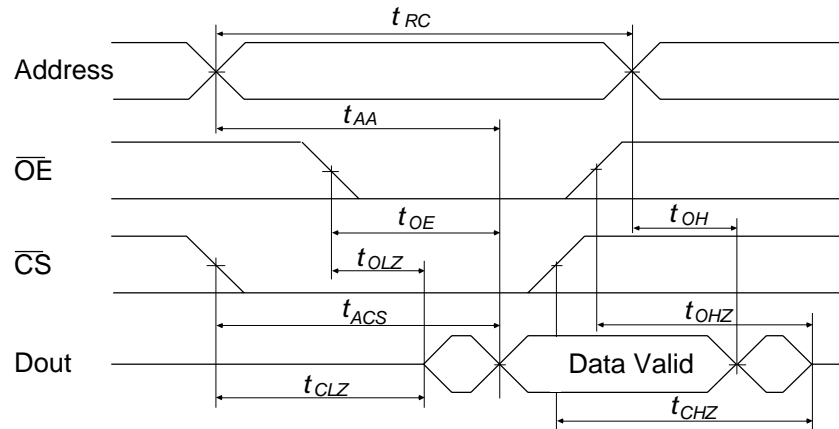


## Electrical Characteristics & Recommended AC Operating Conditions

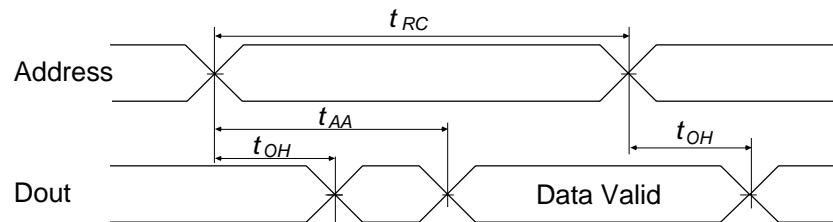
### Read Cycle

Parameter	Symbol	-35		-45		-55		Unit
		min	max	min	max	min	max	
Read Cycle Time	$t_{RC}$	35	-	45	-	55	-	ns
Address Access Time	$t_{AA}$	-	35	-	45	-	55	ns
Chip Select Access Time	$t_{ACS}$	-	35	-	45	-	55	ns
Output Enable to Output Valid	$t_{OE}$	-	18	-	23	-	25	ns
Output Hold From Address Change	$t_{OH}$	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z <sup>(1)</sup>	$t_{CLZ}$	10	-	10	-	10	-	ns
Output Enable to Output in Low Z <sup>(1)</sup>	$t_{OLZ}$	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z <sup>(1)</sup>	$t_{CHZ}$	0	20	0	20	0	20	ns
Output Disable to Output in High Z <sup>(1)</sup>	$t_{OHZ}$	0	10	0	15	0	20	ns

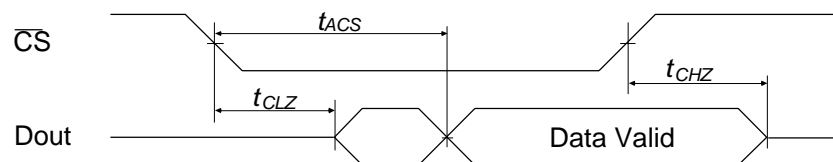
### Read Cycle 1 Timing Waveform <sup>(1,2)</sup>



### Read Cycle 2 Timing Waveform <sup>(1,2,3,5)</sup>



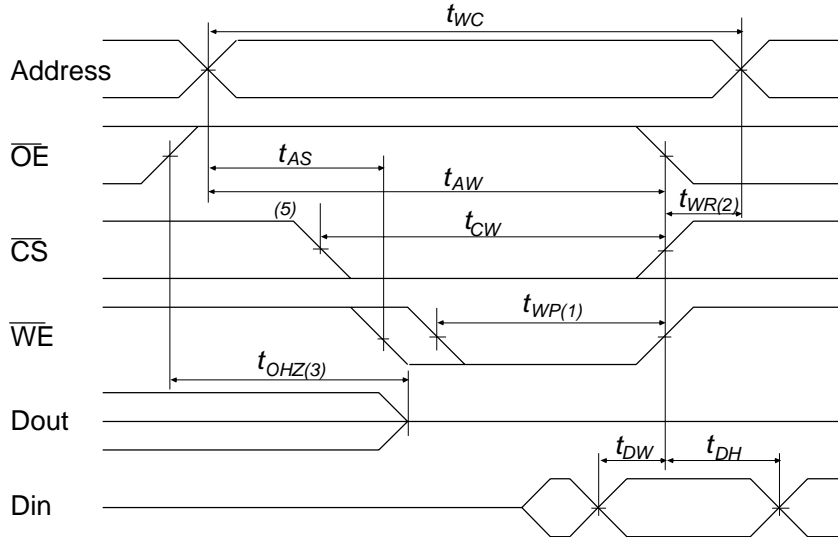
### Read Cycle 3 Timing Waveform <sup>(1,2,4,5)</sup>



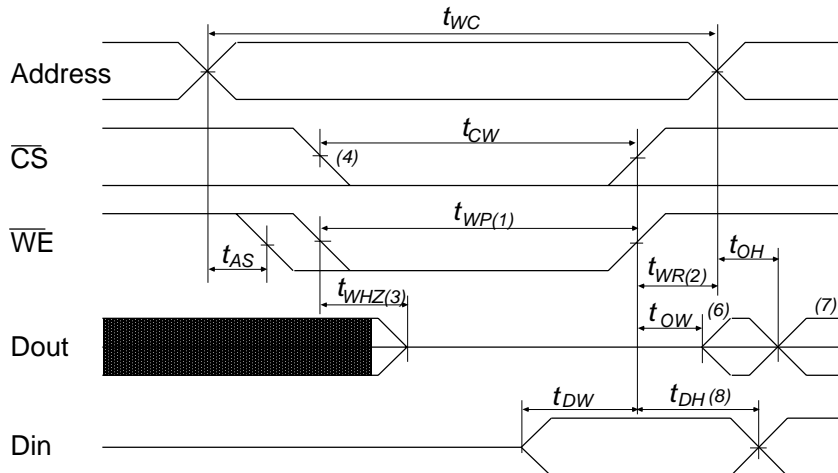
- Notes: (1)  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.  
 (2)  $\overline{OE}$  is High throughout a Read Cycle.  
 (3) Device is continuously selected, while  $\overline{CS}=v_{IL}$ .  
 (4) Address valid prior to or coincident with  $\overline{CS}$  transition low.  
 (5)  $\overline{OE}=V_{IL}$

**Write Cycle**

Parameter	Symbol	-35		-45		-55		Unit
		min	max	min	max	min	max	
Write Cycle Time	$t_{WC}$	35	-	45	-	55	-	ns
Chip Selection to End of Write	$t_{CW}$	30	-	40	-	50	-	ns
Address Valid to End of Write	$t_{AW}$	30	-	40	-	50	-	ns
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	25	-	30	-	40	-	ns
Write Recovery Time	$t_{WR}$	3	-	3	-	3	-	ns
Data Valid to End of Write <sup>(9)</sup>	$t_{WHZ}$	0	10	0	15	0	20	ns
Data Valid to End of Write	$t_{DW}$	20	-	25	-	30	-	ns
Data Hold Time	$t_{DH}$	0	-	0	-	0	-	ns
Write Enabled to Output in High Z <sup>(9)</sup>	$t_{OHZ}$	0	10	0	15	0	20	ns
Write Cycle 1 (WE Controlled) Output Active from End of Write <sup>(9)</sup>	$t_{OW}$	0	-	0	-	0	-	ns



**Write Cycle 2<sup>(5)</sup>**



## AC Characteristics Notes

- (1) A write occurs during the overlap ( $t_{wP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
- (2)  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
- (3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
- (4) If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  low transition, outputs remain in a high impedance state.
- (5)  $\overline{OE}$  is continuously low. ( $\overline{OE}=V_{IL}$ )
- (6) Dout is in the same phase as written data of this write cycle.
- (7) Dout is the read data of next address.
- (8) If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
- (9)  $t_{WHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

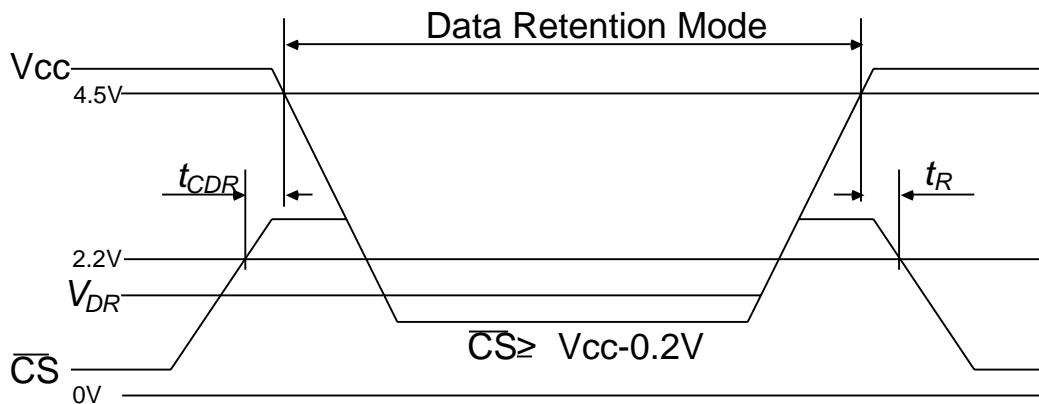
## Low $V_{CC}$ Data Retention Characteristics - L Version Only ( $T_A=0^\circ\text{C}$ to $+70^\circ\text{C}$ )

Parameter	Symbol	Test Condition	min	typ <sup>(2)</sup>	max	Unit
$V_{CC}$ for Data Retention	$V_{DR}$	$\overline{CS} \cdot V_{CC} - 0.2V$	2.0	-	-	V
Data Retention Current	$I_{CCDR}$	$V_{CC}=3.0V, \overline{CS} \cdot 2.8V, 0.2V \cdot V_{IN} \cdot 2.8V$	-	16	800	$\mu\text{A}$
CS high to Data Retention Time	$t_{CDR}$	See Retention Waveform	0	-	-	ns
Operation Recovery Time	$t_R$	See Retention Waveform	$t_{RC}^{(1)}$	-	-	ns

Notes: (1)  $t_{RC}$ =Read Cycle Time.

(2) Typical figures are measured at  $25^\circ\text{C}$ .

## Low $V_{CC}$ Data Retention Waveform - L Version only



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## Ordering Information

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### MS32256FKXLI-45

