TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES

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256K x 8 SRAM MODULE

SYS8256RKX - 55/70/85/10/12

Issue 2.0 : February 1999

Description

The SYS8256RKX is a plastic 2M Static RAM Module housed in a standard 32 pin Single In-Line package organised as 256K x 8. This offers a very high PCB packing density, with the possibility of placing the modules on a 5mm pitch.

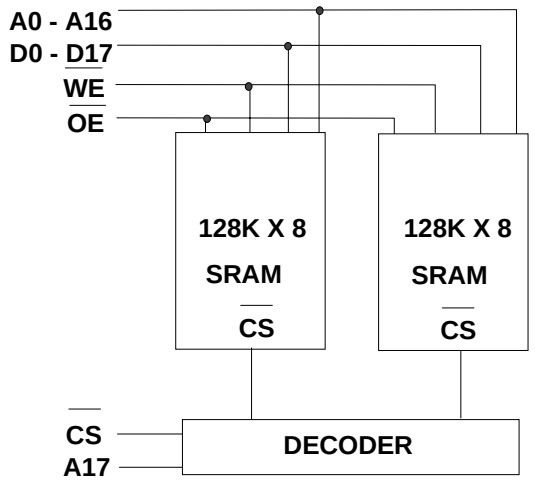
Fast access times of 55 to 85 ns are available as well as standard times of 100 to 120 ns, with the faster modules operating at a slightly higher power consumption.

The SYS8256RKX is offered as standard and low power versions, with the -L module having a low voltage data retention mode.

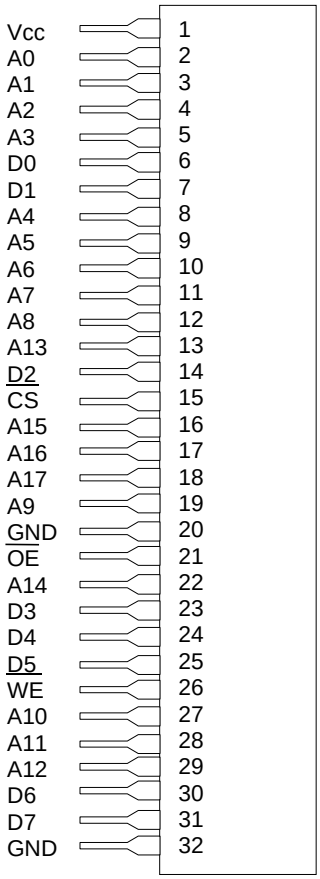
Features

- Access Times of 55/70/85/100/120 ns.
- 32 Pin Single-In-Line package.
- 5 Volt Supply ± 10%.
- Low Power Dissipation:
  Average (min cycle) 566 mW (max).
  Standby (CMOS) 61 mW (max).
- Completely Static Operation.
- Low Voltage V_{CC} Data Retention.
- Directly TTL Compatible.
- On-board Supply Decoupling Capacitors.

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 ~ A17**
Data Input/Output	**D0 ~ D7**
Chip Select Input	**$\overline{CS}$**
Read/Write Input	**$\overline{WE}$**
Output Enable Input	**$\overline{OE}$**
Power (+5V)	**V_{cc}**
Ground	**GND**

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*min*	*typ*	*max*	*unit*
Voltage on any pin relative to GND	V_T	-0.5V	-	+7.0	V
Power Dissipation	P_T	-	1.0	-	W
Storage Temperature	T_{STG}	-55	-	+150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	6.0	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C

DC Electrical Characteristics (V_{CC}=5V±10%) TA 0 to 70°C

Parameter		*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
I/P Leakage Current		I_{LI1}	0V - V_{IN} - V_{CC}	-	-	±4	µA
O/P Leakage Current	D0~D7	I_{Lo}	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to Vcc	-	-	±4	µA
Average Supply Current	55/70/85	I_{CC1}	t_{CYC} = 55ns, $\overline{CS}$ = V_{IL}, V_{IN} = V_{IL}/V_{CC}-2.1V	-	55	103	mA
Average Supply Current	10/12/15	I_{CC2}	t_{CYC} = 100ns, $\overline{CS}$= V_{IL}, V_{IN} =V_{IL}/V_{CC}-2.1V	-	45	70	mA
Standby Supply Current	TTL levels	I_{SB}	$\overline{CS}$ = V_{CC}-2.1V, V_{IL} > V_{IN} > V_{CC}-2.1V	-	7	11	mA
CMOS levels		I_{SB1}	$\overline{CS}$ = V_{CC}-0.2V, 0.2 > V_{IN} > V_{CC}-0.2V	-	0.05	5	mA
-L part, CMOS levels		I_{SB2}	As above	-	10	300	µA
Output Low Voltage		V_{OL}	I_{OL} = 2.1mA	-	-	0.4	V
Output High Voltage		V_{OH}	I_{OH} = -1.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance ($\overline{CS}$, A17)	C_{IN1}	V_{IN} = 0V	8	pF
Input Capacitance (other)	C_{IN2}	V_{IN} = 0V	12	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	16	pF

Data Retention Characteristics - L Version Only

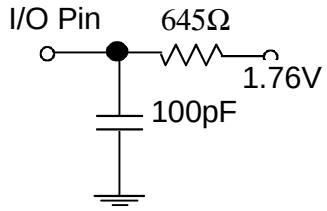
Parameter	*Symbol*	*Test Condition*	*min*	*typ(1)*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$ > V_{CC}-0.2V	2.0	-	-	V
Data Retention Current		V_{CC} = 3.0V, $\overline{CS}$ > V_{CC}-0.2V				
	I_{CCDR1} (2)	T_{OP} = 0°C to 40°C	-	5	100	µA
	I_{CCDR2}	T_{OP} = T_A	-	5	150*(3)*	µA
	I_{CCDR3}	T_{OP} = T_{AI}	-	-	TBA	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes
(1) Typical figures are measured at 25°C.
(2) This parameter is guaranteed not tested.
(3) Maximum figure at 70°C

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

Output Load



AC OPERATING CONDITIONS

Read Cycle

		-55		-70		-85		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	55	-	70	-	85	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	85	ns
Chip Select Access Time	t_{ACS}	-	55	-	70	-	85	ns
Output Enable to Output Valid	t_{OE}	-	30	-	35	-	55	ns
Output Hold from Address Change	t_{OH}	5	-	10	-	10	-	ns
Chip Selection to Output in Low Z (2)	t_{CLZ}	5	-	10	-	10	-	ns
Output Enable to Output in Low Z (2)	t_{OLZ}	5	-	5	-	5	-	ns
Chip Deselection to O/P in High Z (2)	t_{CHZ}	0	20	0	25	0	30	ns
Output Disable to Output in High Z (2)	t_{OHZ}	0	20	0	25	0	30	ns

Read Cycle

		-10		-12		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	100	-	120	-	ns
Address Access Time	t_{AA}	-	100	-	120	ns
Chip Select Access Time	t_{ACS}	-	100	-	120	ns
Output Enable to Output Valid	t_{OE}	-	60	-	70	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	ns
Chip Selection to Output in Low Z (2)	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low Z (2)	t_{OLZ}	5	-	5	-	ns
Chip Deselection to O/P in High Z (2)	t_{CHZ}	0	35	0	45	ns
Output Disable to Output in High Z (2)	t_{OHZ}	0	35	0	45	ns

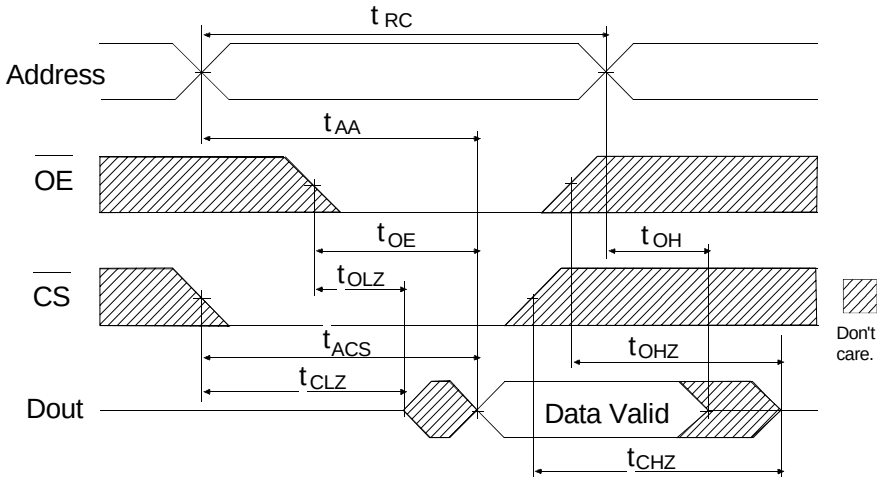
Write Cycle

		-55		-70		-85		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time	t_{WC}	55	-	70	-	85	-	ns
Chip Selection to End of Write	t_{CW}	50	-	60	-	80	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	80	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	40	-	50	-	65	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	5	-	ns
Write to Output in High Z (11)	t_{WHZ}	02	0	0	25	0	30	ns
Data to Write Time Overlap	t_{DW}	30	-	35	-	35	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output active from end of write (10)	t_{OW}	5	-	5	-	5	-	ns

Write Cycle

		-10		-12		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time	t_{WC}	100	-	120	-	ns
Chip Selection to End of Write	t_{CW}	90	-	100	-	ns
Address Valid to End of Write	t_{AW}	90	-	100	-	ns
Address Setup Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	75	-	85	-	ns
Write Recovery Time	t_{WR}	5	-	10	-	ns
Write to Output in High Z (11)	t_{WHZ}	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	40	-	45	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	ns
Output active from end of write (10)	t_{OW}	5	-	5	-	ns

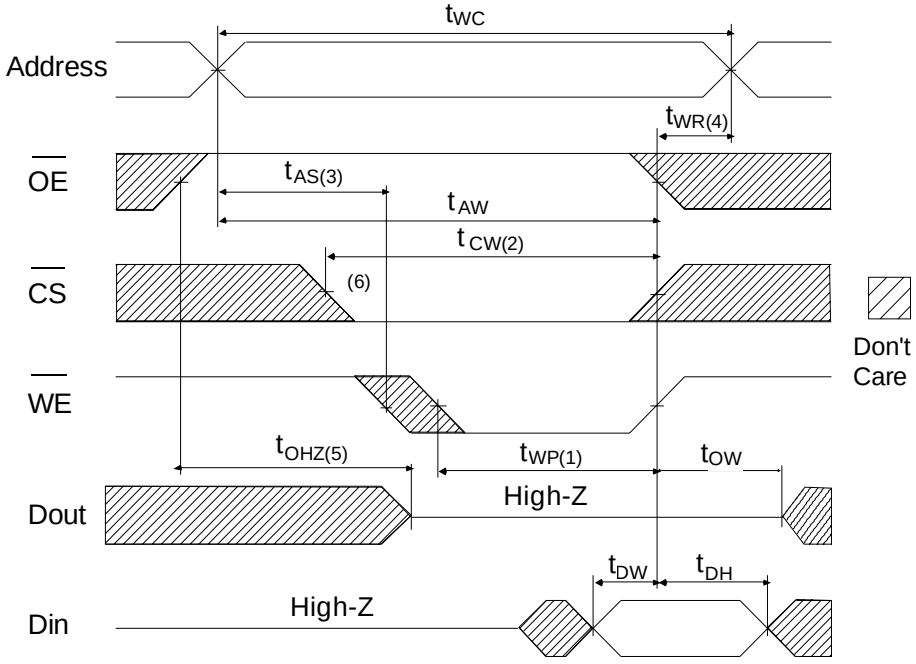
Read Cycle Timing Waveform



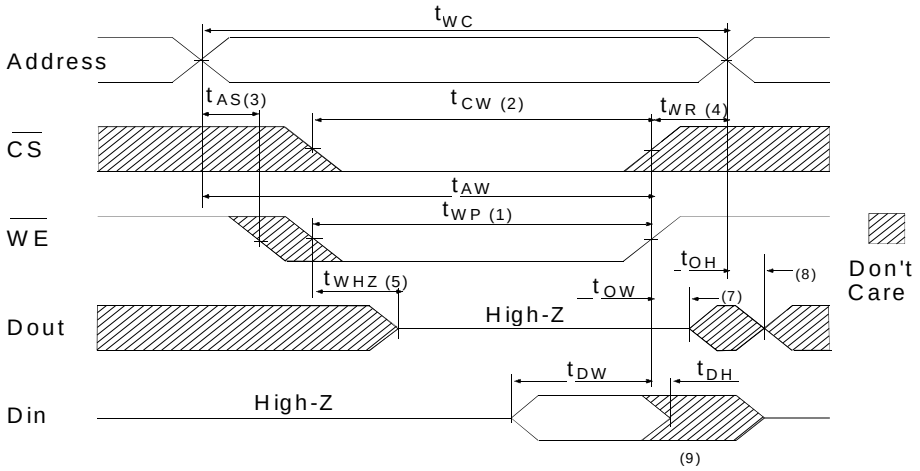
Notes (1) $\overline{WE}$ is High for Read Cycle.

(2) t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform



AC Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(2) t_{CW} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(3) t_{AS} is measured from the address valid to the beginning of write.

(4) t_{WR} is measured from the earliest of $\overline{CS}$ or $\overline{WE}$ going high to the end of write.

(5) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(6) If $\overline{CS}$ goes low simultaneously with WE going low or after $\overline{WE}$ going low , outputs remain in a high impedance state.

(7) D_{OUT} is in the same phase as written data of this write cycle.

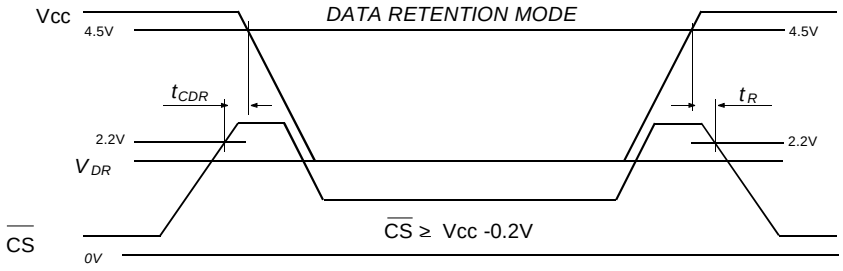
(8) D_{OUT} is the read data of next address.

(9) If $\overline{CS}$ is low during this period, I/O pins are in the output state, and inputs out of phase must not be applied to I/O pins.

(10) This parameter is sampled and not 100% tested.

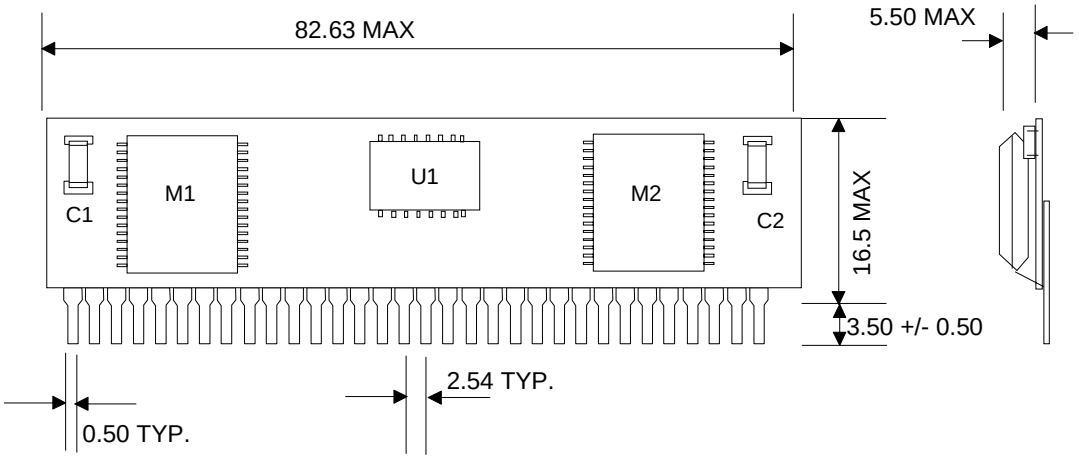
(11) t_{WHZ} is defined as the time at which the outputs achieve open circuit conditions and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.

Data Retention Waveform



Package Information

32 Pin SIP



Dimensions in mm

Ordering Information

SYS8256RKXLI - 10

Speed	55	=	55 ns (Commercial only)
	70	=	70 ns
	85	=	85 ns
	10	=	100 ns
	12	=	120 ns
Temperature Range	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
Power Consumption	Blank	=	Standard Part
	L	=	Low Power Part
Package	RKX	=	Plastic 32 pin SIL
Organization	8256	=	256K x 8
Memory Type	SYS	=	Static RAM

I-55 parts are not available at present