

# TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES



## 1M x 8 SRAM MODULE

### SYS81000FKX - 70/85/10/12

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#### Description

The SYS81000FKX is a plastic 8 Mbit Static RAM Module housed in a JEDEC standard 36 pin Dual In-Line package organised as 1M x8.

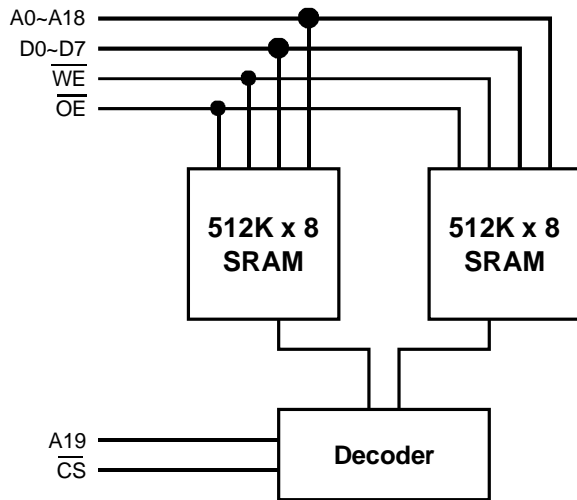
The module utilises SRAM's housed in TSOP II packages, and uses single sided surface mount techniques, buried decoder and dual board construction to achieve a very high density module.

Fast access times of 70 to 120ns are available. The  $\overline{OE}$  pin allows faster access times than address access during a read cycle. Low voltage data retention mode available ( -L Version only).

#### Features

- Access Times of 70/85/100/120 ns.
- 36 Pin JEDEC standard Dual-In-Line package.
- 5 Volt Supply  $\pm 10\%$ .
- Low Power Dissipation:  
Average (min cycle) 565mW (max).  
Standby (-L Part CMOS) 3mW (max).
- Completely Static Operation.
- Low Voltage  $V_{CC}$  Data Retention.
- Directly TTL Compatible.
- On-board Supply Decoupling Capacitors.

#### Block Diagram



#### Pin Definition

Pin	Signal	Pin	Signal
A0	1	36	NC
A1	2	35	A19
A2	3	34	A18
A3	4	33	A17
A4	5	32	A16
CS	6	31	OE
D0	7	30	D7
D1	8	29	D6
Vcc	9	28	GND
GND	10	27	Vcc
D2	11	26	D5
D3	12	25	D4
WE	13	24	A15
A5	14	23	A14
A6	15	22	A13
A7	16	21	A12
A8	17	20	A11
A9	18	19	A10

TOP VIEW

#### Pin Functions

Address Inputs	A0 ~ A19
Data Input/Output	D0 ~ D7
Chip Select	$\overline{CS}$
Write Enable	$\overline{WE}$
Output Enable	$\overline{OE}$
Power (+5V)	$V_{CC}$
Ground	GND

#### Package Details

Plastic 36 pin 0.6" Jedec DIP

**DC OPERATING CONDITIONS****Absolute Maximum Ratings** <sup>(1)</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Voltage on any pin relative to $V_{SS}$	$V_T^{(2)}$	-0.3	-	7.0	V
Power Dissipation	$P_T$	-	1.0	-	W
Storage Temperature	$T_{STG}$	-55	-	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2)  $V_T$  can be -3.0V pulse of less than 30ns.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	-	0.8	V
Operating Temperature (Commercial)	$T_A$	0	-	70	°C
(Industrial)	$T_{AI}$	-40	-	85	°C

**DC Electrical Characteristics** ( $V_{CC}=5V\pm 10\%$ )  $T_A$  0 to 70 °C

Parameter	Symbol	Test Condition	Min	Typ	max	Unit
I/P Leakage Current Address, $\overline{OE}$ , $\overline{WE}$	$I_{LI}$	$0V \leq V_{IN} \leq V_{CC}$	-3	-	3	$\mu A$
Output Leakage Current	$I_{LO}$	$\overline{CS} = V_{IH}$ , $V_{IO} = GND$ to $V_{CC}$ , $\overline{OE} = V_{IH}$	-3	-	3	$\mu A$
Operating Supply Current	$I_{CC1}$	Min. Cycle, $\overline{CS} = V_{IL}$ , $V_{IL} \leq V_{IN} \leq V_{IH}$	-	-	103	mA
Standby Supply Current	TTL levels	$\overline{CS} = V_{IH}$	-	-	6	mA
	CMOS levels	$\overline{CS} \geq V_{CC}-0.2V$ , $0.2 \leq V_{IN} \leq V_{CC}-0.2V$	-	-	1	mA
	-L Version (CMOS)	$\overline{CS} \geq V_{CC}-0.2V$ , $0.2 \leq V_{IN} \leq V_{CC}-0.2V$	-	-	500	$\mu A$
Output Voltage	$V_{OL}$	$I_{OL} = 2.1mA$	-	-	0.4	V
	$V_{OH}$	$I_{OH} = -1.0mA$	2.4	-	-	V

Typical values are at  $V_{CC}=5.0V$ ,  $T_A=25^\circ C$  and specified loading.

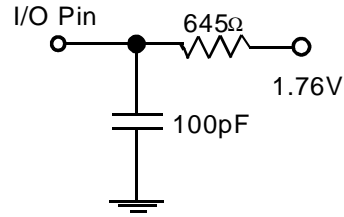
**Capacitance** ( $V_{CC}=5V\pm 10\%$ ,  $T_A=25^\circ C$ )

Note: Capacitance calculated, not measured.

Parameter	Symbol	Test Condition	max	Unit
Input Capacitance (Address, $\overline{OE}$ , $\overline{WE}$ )	$C_{IN1}$	$V_{IN} = 0V$	22	pF
I/P Capacitance (other)	$C_{IN2}$	$V_{IN} = 0V$	10	pF
I/O Capacitance	$C_{IO}$	$V_{IO} = 0V$	16	pF

**AC Test Conditions** **Output Load**

- \* Input pulse levels: 0V to 3.0V
- \* Input rise and fall times: 5ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: see diagram
- \*  $V_{CC} = 5V \pm 10\%$



**Operation Truth Table**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DATA PINS	SUPPLY CURRENT	MODE
H	X	X	High Impedance	$I_{SB1}, I_{SB2}, I_{SB3}$	Standby
L	L	H	Data Out	$I_{CC1}$	Read
L	H	L	Data In	$I_{CC1}$	Write
L	L	L	Data In	$I_{CC1}$	Write
L	H	H	High-Impedance	$I_{SB1}, I_{SB2}, I_{SB3}$	High-Z

Notes : H =  $V_{IH}$  : L =  $V_{IL}$  : X =  $V_{IH}$  or  $V_{IL}$

**Low  $V_{CC}$  Data Retention Characteristics - L Version Only**

Parameter	Symbol	Test Condition	min	typ <sup>(1)</sup>	max	Unit
$V_{CC}$ for Data Retention	$V_{DR}$	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	-	V
Data Retention Current	$I_{CCDR1}$	$3.0 \leq V_{CC} \leq 5.5V, \overline{CS} \geq V_{CC} - 0.2$	-	-	180	$\mu A$
Chip Deselect to Data Retention Time	$t_{CDR}$	See Retention Waveform	0	-	-	ns
Operation Recovery Time	$t_R$	See Retention Waveform	5	-	-	ms

- Notes (1) Typical figures are measured at 25°C.  
 (2) This parameter is guaranteed not tested.

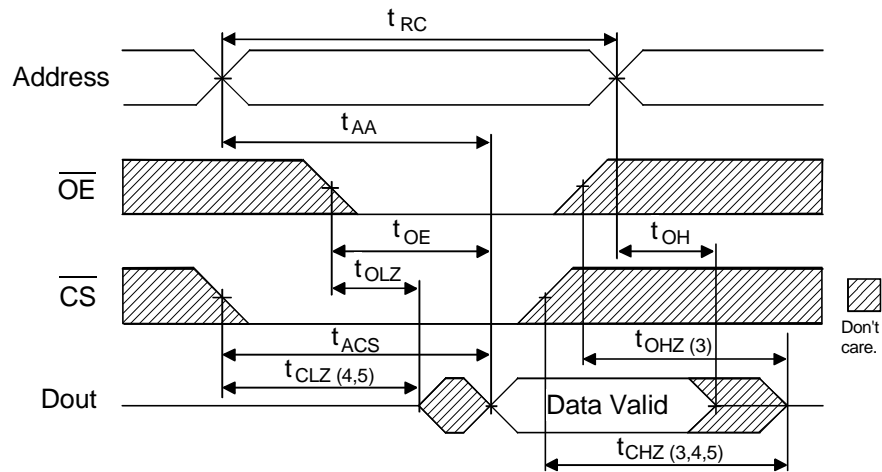
**AC OPERATING CONDITIONS****Read Cycle**

Parameter	Symbol	-70		-85		-10		-12		Unit
		min	max	min	max	min	max	min	max	
Read Cycle Time	$t_{RC}$	70	-	85	-	100	-	120	-	ns
Address Access Time	$t_{AA}$	-	70	-	85	-	100	-	120	ns
Chip Select Access Time	$t_{ACS}$	-	70	-	85	-	100	-	120	ns
Output Enable to Output Valid	$t_{OE}$	-	40	-	45	-	50	-	55	ns
Output Hold from Address Change	$t_{OH}$	10	-	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z	$t_{CLZ}$	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	$t_{OLZ}$	5	-	5	-	5	-	5	-	ns
Chip Deselection to O/P in High Z	$t_{CHZ}$	0	25	0	30	0	35	0	40	ns
Output Disable to Output in High Z	$t_{OHZ}$	0	25	0	30	0	35	0	40	ns

**Write Cycle**

Parameter	Symbol	-70		-85		-10		-12		Unit
		min	max	min	max	min	max	min	max	
Write Cycle Time	$t_{WC}$	70	-	85	-	100	-	120	-	ns
Chip Selection to End of Write	$t_{CW}$	60	-	70	-	80	-	100	-	ns
Address Valid to End of Write	$t_{AW}$	60	-	70	-	80	-	100	-	ns
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	50	-	60	-	70	-	80	-	ns
Write Recovery Time	$t_{WR}$	3	-	3	-	3	-	3	-	ns
Write to Output in High Z	$t_{WHZ}$	0	25	0	30	0	35	0	40	ns
Data to Write Time Overlap	$t_{DW}$	30	-	35	-	40	-	45	-	ns
Data Hold from Write Time	$t_{DH}$	0	-	0	-	0	-	0	-	ns
Output active from End of Write	$t_{OW}$	3	-	3	-	3	-	3	-	ns

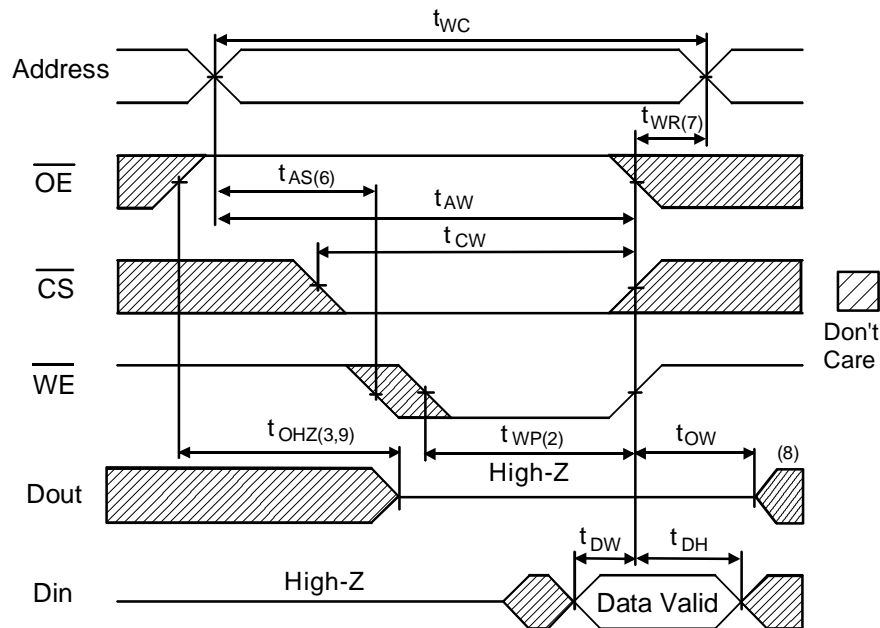
**Read Cycle Timing Waveform** <sup>(1,2)</sup>



**AC Read Characteristics Notes**

- (1)  $\overline{WE}$  is High for Read Cycle.
- (2) All read cycle timing is referenced from the last valid address to the first transition address.
- (3)  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.
- (4) At any given temperature and voltage condition,  $t_{CHZ}$  (max) is less than  $t_{CLZ}$  (min) both for a given module and from module to module.
- (5) These parameters are sampled and not 100% tested.

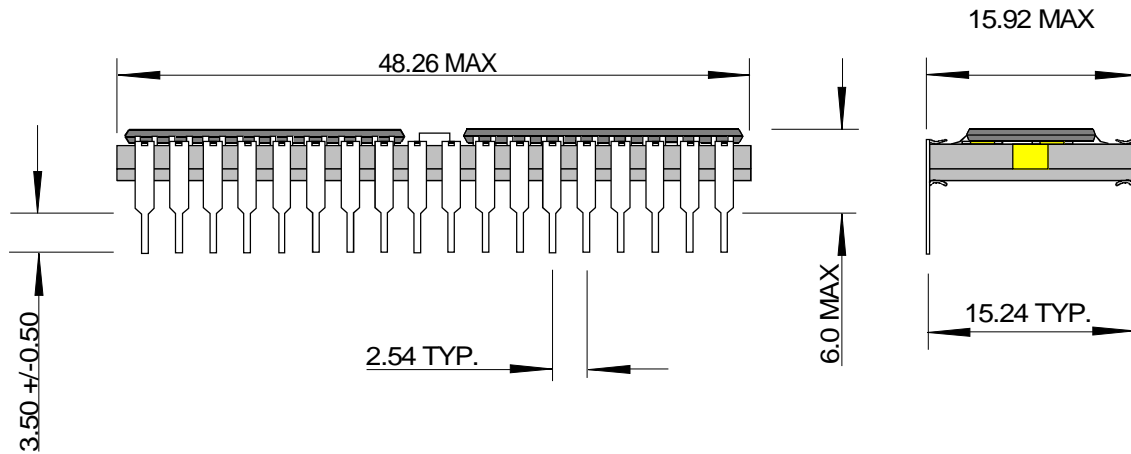
**Write Cycle No.1 Timing Waveform** <sup>(1,4)</sup>





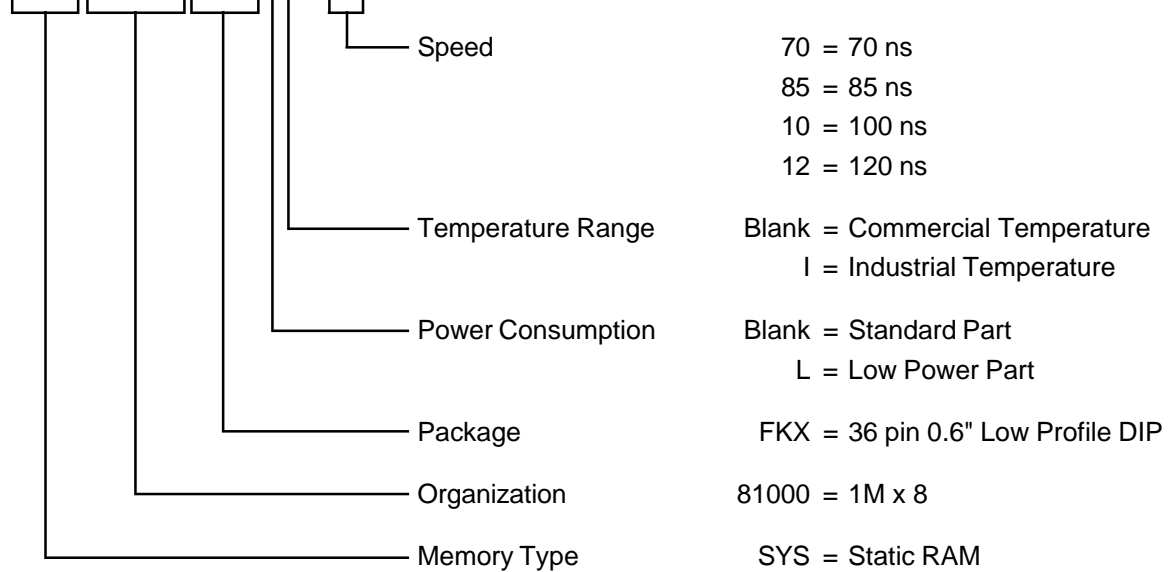
**Package Information**      Dimensions in mm

**Plastic 36 Pin 0.6" Dual-In-Line Low Profile.**



**Ordering Information**

**SYS81000FKXLI - 70**



**Note :**

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