

TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES



64K x 16 SRAM MODULE

SYS1664FK-70/85/10/12

Elm Road, West Chirton Industrial Estate, North Shields,
NE29 8SE, ENGLAND. TEL +44 191 2930519. FAX +44 191 2590997

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Description

The SYS1664FK is a plastic 1M Static RAM Module housed in a standard 40 pin Dual-In-Line package organised as 64K x 16 with access times of 70, 85, 100, or 120 ns. The device has on-board decoding and capacitors.

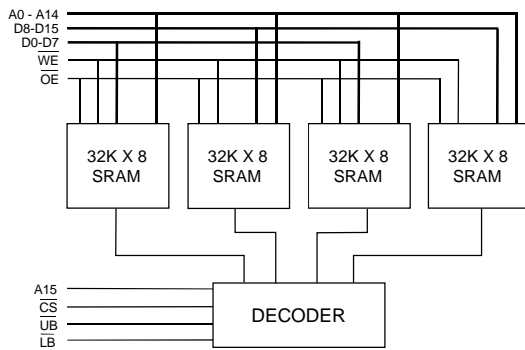
The module is constructed using four 32Kx8 SRAMs in SOP packages mounted onto both sides of an FR4 epoxy substrate. This offers an extremely high PCB packing density.

The device is offered in standard and low power versions, with the -L module having a low voltage data retention mode for battery backed applications.

Features

- Access Times of 70/85/100/120 ns.
- Low Power Disipation:
 - Operating (16 bit mode) 1.6 W (Max)
 - Standby -L CMOS 1.38 mW (Max)
- Upper and Lower Byte Select Control
- Completely Static Operation.
- Equal Access and Cycle Times.
- Low Voltage V_{CC} Data Retention -L version.
- Directly TTL Compatible.
- 5 Volt Supply $\pm 10\%$.
- JEDEC approved 40 Pin Dual-In-Line package.

Block Diagram



Pin Definition

A15	1	40	V_{CC}
CS	2	39	\overline{WE}
D15	3	38	\overline{UB}
D14	4	37	\overline{LB}
D13	5	36	A14
D12	6	35	A13
D11	7	34	A12
D10	8	33	A11
D9	9	32	A10
D8	10	31	A9
GND	11	30	GND
D7	12	29	A8
D6	13	28	A7
D5	14	27	A6
D4	15	26	A5
D3	16	25	A4
D2	17	24	A3
D1	18	23	A2
D0	19	22	A1
OE	20	21	A0

Pin Functions

Address Inputs	A0 - A15
Data Input/Output	D0 - D15
Chip Select	\overline{CS}
Write Enable	\overline{WE}
Output Enable	\overline{OE}
Upper Byte Select	\overline{UB}
Lower Byte Select	\overline{LB}
Power (+5V)	V_{CC}
Ground	GND

Package Details

Plastic 40 Pin 0.6" DIL

Absolute Maximum Ratings ⁽¹⁾

Voltage on any pin relative to V_{SS}	V_T	-0.5V to +7	V
Power Dissipation	P_T	1.6	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of The device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse Width:-1.0V for 50ns

Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (1664I)

DC Electrical Characteristics ($T_A=-40$ to $+85^\circ\text{C}$, $V_{CC}=5V\pm 10\%$.)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{IL}	$V_{IN}=0V$ to V_{CC}	-	-	± 8	μA
Output Leakage Current	I_{OL}	$V_{IO}=\text{Gnd}$ to V_{CC}	-	-	± 8	μA
Average Supply Current ⁽¹⁾	I_{CC1}	Min. Cycle,duty=100%, $I_{IO}=0\text{mA}$	-	-	70	mA
	I_{CC2}	Min. Cycle,duty=100%, $I_{IO}=0\text{mA}$	-	-	140	mA
Standby Supply Current	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{IN}\geq 0V$	-	-	8	mA
	I_{SB2}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{IN}\geq 0V$	-	-	250	μA
Input Low Voltage ⁽²⁾	V_{IL}		-0.3	-	0.8	V
Input High Voltage ⁽³⁾	V_{IH}		2.2	-	$V_{CC}+0.3$	V
Output Low Voltage	V_{OL}	$I_{OL}=2.1\text{mA}$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH}=-400\mu\text{A}$	2.4	-	-	V

Notes (1) For these currents min and max values are given for 8 and 16 bit mode operation respectively. Each individual value shown is a maximum.

(2) -1.0V for pulse width - 50 ns

(3) $V_{CC}+1.5V$ for -20 ns. If V_{IH} is over the specified max. value, READ operation cannot be guaranteed.

Capacitance ($V_{CC}=5V\pm 10\%$, $T_A=25^\circ\text{C}$)

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance:	C_{IN}	$V_{IN}=0V$	-	40	pF
I/O Capacitance:	C_{IO}	$V_{IO}=0V$	-	40	pF

Note: This parameter is calculated not measured.

AC Test Conditions

- * Input pulse levels: 0V to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: 1 TTL gate + 100pF
- * $V_{CC}=5V\pm 10\%$

Operation Truth Table

\overline{CS}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	Mode	Outputs	Supply Current
H	X	X	X	X	Standby	High Z (D0-D15)	I _{sb1} , I _{sb2}
L	X	X	H	H	Standby	HighZ (D0-D15)	I _{sb1} , I _{sb2}
L	L	H	H	L	Read 8bit	Dout (8-15)	I _{cc1}
L	L	H	L	H	Read 8bit	Dout (0-7)	I _{cc1}
L	L	H	L	L	Read 16bit	Dout (0-15)	I _{cc2}
L	X	L	H	L	Write 8bit	Din (8-15)	I _{cc1}
L	X	L	L	H	Write 8bit	Din(0-7)	I _{cc1}
L	X	L	L	L	Write 16bit	Din (0-15)	I _{cc2}
L	H	H	L	L	Output Disable	High Z (D0-D15)	I _{cc2}
L	H	H	H	L	Output Disable	High Z (D0-D15)	I _{cc2}
L	H	H	L	H	Output Disable	High Z (D0-D15)	I _{cc2}

Notes : H = V_{IH} : L = V_{IL} : X = V_{IH} or V_{IL}

Low V_{CC} Data Retention Characteristics - L Version Only

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	-	V
Data Retention Current	I_{CCDR1}	$V_{CC}=3.0V, \overline{CS} \geq 2.8V, T_{OP}=T_A$	-	280	380	μA
	I_{CCDR2}	$V_{CC}=3.0V, \overline{CS} \geq 2.8V, T_{OP}=T_{AI}$	-	-	460	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	$t_{RC}^{(1)}$	-	-	ns

Notes: (1) t_{RC} =Read Cycle Time

AC OPERATING CONDITIONS

Read Cycle

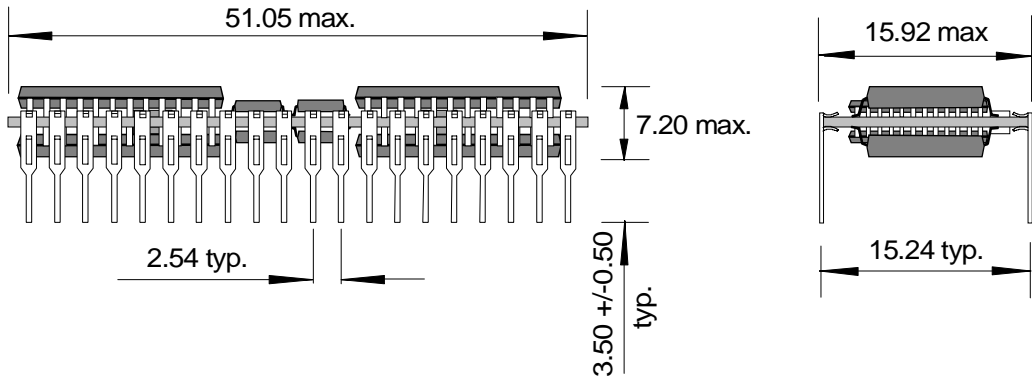
Parameter	Symbol	-70		-85		-10		-12		Unit
		min	max	min	max	min	max	min	max	
Read Cycle Time	t_{RC}	70	-	85	-	100	-	120	-	ns
Address Access Time	t_{AA}	-	70	-	85	-	100	-	120	ns
Chip Select Access Time	t_{ACS}	-	70	-	85	-	100	-	120	ns
Output Enable to Output Valid	t_{OE}	-	35	-	45	-	50	-	60	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	30	0	35	0	40	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	30	0	35	0	40	ns

Write Cycle

Parameter	Symbol	-70		-85		-10		-12		Unit
		min	max	min	max	min	max	min	max	
Write Cycle Time	t_{WC}	70	-	85	-	100	-	120	-	ns
Chip Selection to End of Write	t_{CW}	65	-	70	-	80	-	85	-	ns
Address Valid to End of Write	t_{AW}	65	-	70	-	80	-	85	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	55	-	60	-	70	-	80	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	25	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	30	-	35	-	40	-	50	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	30	0	35	0	40	ns
Output Active from End of Write	t_{OW}	10	-	10	-	10	-	10	-	ns

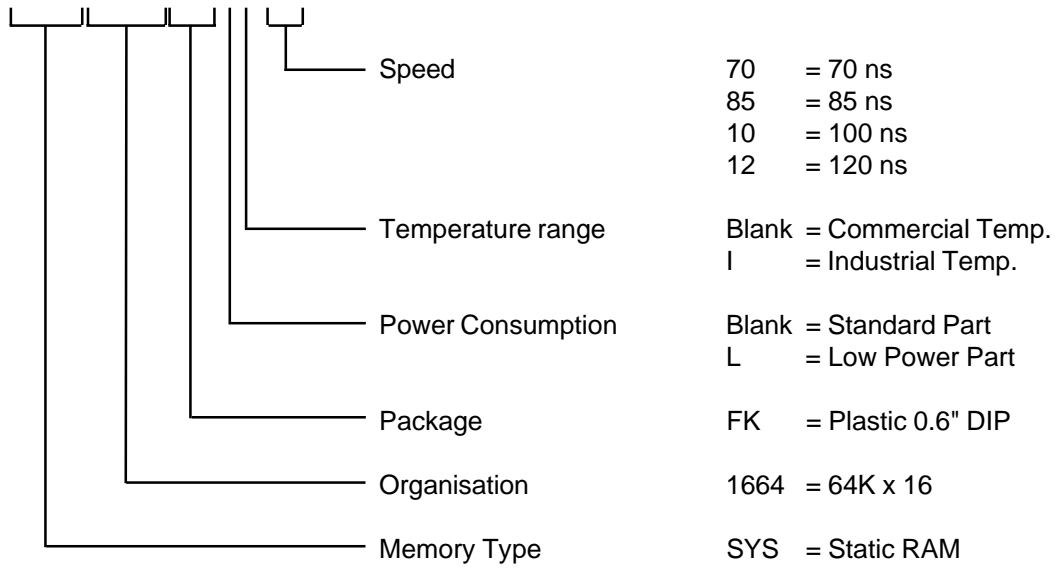
Package Details. Dimensions in mm(inches)

40 Pin 0.6" Dual-In-Line Package.



Ordering Information

SYS1664FKLI-10



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